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10/574,775	04/06/2006	Sougo Ohta	071971-0460	2530

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EXAMINER	
HSIEH, HSIN YI	

ART UNIT	PAPER NUMBER
2811	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/574,775	OHTA ET AL.	
	Examiner	Art Unit	
	Hsin-Yi (Steven) Hsieh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-13 and 15-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-13 and 15-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 February 2008* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 07/27/2009 has been entered.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the feature of "a microlens" recited in claims 19 and 23 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the

renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claim 16, 17, 20 and 21** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 16 and 20 recite the limitation "a first output interconnect formed as a first-level metal interconnect; and a second output interconnect formed as a second-level metal interconnect" in the last three lines of the claims 16 and 20, which lacks the support the original presentation. The only elements which is related to the first and second **output** interconnects is the output interconnect 211 (Fig. 3, paragraph [0057-0058]) and there is no discourse in the original presentation stating that the output interconnect 211 is formed as a first-level metal interconnect or a second-level metal interconnect. Claims 17 and 21 are rejected because they depend on the rejected claims 16 and 20.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. **Claim 8-13, 15-23** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 8 recites the limitation "the upper left corner" in the 13th line of the claim. There is insufficient antecedent basis for this limitation in the claim.

8. Claim 8 recites the limitation "the plane" in the 13th line of the claim. There is insufficient antecedent basis for this limitation in the claim.

9. Claim 15 recites the limitation "the longest edge" in the last line of the claim. There is insufficient antecedent basis for this limitation in the claim.

10. Claim 15 recites the limitation "the longest edge of each of the first transfer transistor and the amplifier transistor." in the last line of the claim. This limitation is ambiguous due to the lack of definitions of the first transfer transistor and the amplifier transistor. The first transfer transistor and the amplifier transistor of the instant application are MOS transistors which generally include at least the source region, the drain region, the gate electrode, and the channel region. In a more complicated structure, one element of the MOS transistors might be shared by other distinct element which makes defining the boundary of MOS transistors a necessity to avoid the ambiguity. For example, the photodiode of the instant application can be considered as a part of the transfer transistor because it is the source/drain of the transfer transistor, while the photodiode can also be considered not a part of the transfer transistor due to its function as an

image sensor. The ambiguity caused by the lack of definitions of the transfer transistor and the amplifier transistor renders the limitation indefinite.

11. Claims 19 and 23 recite the limitation "the photodiode" in the last line of claims 19 and 23. It is unclear the limitation refers to the first photodiode or the second photodiode recited in claims 8 and 15.

12. Claims 9-13, 16-18, and 20-23 are rejected because they depend on the rejected claims 8 and 15.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. **Claims 8-13 and 15** are rejected under 35 U.S.C. 102(b) as being anticipated by Guidash (US 6,657,665 B1) as can be understood since claims 8-13 and 15-23 have been rejected under 35 U.S.C. 112.

15. Regarding **claim 8**, Guidash teaches a solid-state imaging apparatus (image sensor; Abstract) comprising: a substrate (semiconductor substrate; Abstract); a first pixel (pixel 50 of column 1 and row B; Fig. 6, col. 5 line 26) formed on the substrate (Abstract) including a first photodiode (52 in the first pixel; Fig. 6, col. 5 line 26), a first transfer transistor (the transistor formed with the transfer gate 23 in the first pixel; Fig. 6, col. 5 line 58) and a first floating diffusion (46 in the first pixel; Fig. 6, col. 5 line 21); a second pixel (pixel 50 of column 1 and

row C; Fig. 6, col. 5 line 26) formed on the substrate (Abstract) adjacent to the first pixel (50 of column 1 and row B) including a second photodiode (52 in the second pixel; Fig. 6, col. 5 line 26), a second transfer transistor (the transistor formed with the transfer gate 23 in the second pixel; Fig. 6, col. 5 line 58) and a second floating diffusion (46 in the second pixel; Fig. 6, col. 5 line 21); a reset transistor (14; Fig. 6, col. 5 line 19) formed on the substrate (Abstract); and an amplifier transistor (source follower input signal transistor 21; Fig. 6, col. 5 lines 19-20) formed on the substrate (abstract), wherein a gate electrode (22; Fig. 6, col. 5 line 24) of the amplifier transistor (21) is connected to the first floating diffusion (46 in the first pixel; see Fig. 6 and col. 5, lines 21-24) and the second floating diffusion (46 in the second pixel; see Fig. 6 and col. 5, lines 21-24), a source (16; Fig. 6, col. 5 line 23) of the reset transistor (14) is connected to the first floating diffusion (46 in the first pixel; see Fig. 6 and col. 5, lines 21-24) and the source (16) of the reset transistor (14) is connected to the second floating diffusion (46 in the second pixel; see Fig. 6 and col. 5, lines 21-24), and using the upper left comer with respect to the plane of the substrate (i.e. the plane of the paper of Fig. 6 which corresponds to the upper plane of the substrate shown in Fig. 1) of each of the first pixel (50 of column 1 and row B) and the second pixel (50 of column 1 and row C) as a reference point, the first photodiode (52 in the first pixel) and second photodiode (52 in the second pixel) are substantially equal in shape (see Fig. 6) and intra-pixel location (the photodiode 52 location with respect to the upper left corner of pixel 50; see Fig. 6), and the first floating diffusion (46 in the first pixel) and second floating diffusion (46 in the second pixel) are substantially equal in size (see Fig. 6) and intra-pixel location (the floating diffusion 46 location with respect to the upper left corner of pixel 50; see Fig. 6).

16. Regarding **claim 9**, Guidash also teaches the solid-state imaging apparatus of claim 8, further comprising: a power supply interconnect (VDD contact in Fig. 6, i.e. voltage supply 8 in Fig. 4; Fig. 6, col. 3 line 60); and an output interconnect (the source/drain contact of the row select gate transistor 30 with a row select gate (RSG) 31; Fig. 6, col. 3 line 62), wherein the power supply interconnect (8 or VDD contact) is connected to a drain (the upper source/drain region) of the reset transistor (14; see Fig. 6) and a source (the lower source/drain) of the amplifier transistor (21; see Fig. 6), and the output interconnect (the source/drain contact of the 30) is connected to a drain (the upper source/drain region) of the amplifier transistor (21; they are electrically connected through the channel of the row select gate transistor 30, see Fig. 6).

17. Regarding **claim 10**, Guidash also teaches the solid-state imaging apparatus of claim 8, wherein the amplifier transistor (21) is formed in the first pixel (pixel 50 of column 1 and row B), the reset transistor (14) is formed in the second pixel (pixel 50 of column 1 and row C, see Fig. 6), and a distance and direction (a distance in the horizontal direction) from the first photodiode (PD1b in Fig. 6) to the amplifier transistor (21; the distance between the right end of PD1b and the right end of the gate of 21) are substantially equal to a distance and direction (a distance in the horizontal direction) from the second photodiode (PD1c in Fig. 6) to the reset transistor (14; the distance between the right end of PD1c and the right end of the gate of 14).

18. Regarding **claim 11**, Guidash also teaches the solid-state imaging apparatus of claim 8, wherein a shape and size of the first pixel (pixel 50 of column 1 and row B) are substantially equal to a shape and size as that of the second pixel (pixel 50 of column 1 and row C; see Fig. 6).

19. Regarding **claim 12**, Guidash also teaches the solid-state imaging apparatus of claim 8, wherein the solid-state imaging apparatus (Fig. 6) comprises a plurality of units (the unit of two

pixels 50s of column 1 and rows B and C shown in Fig. 6), and each of the units includes only the first pixel (50 of column 1 and row B), the second pixel (50 of column 1 and row C), the reset transistor (14) and the amplifier transistor (21).

20. Regarding **claim 13**, Guidash also teaches the solid-state imaging apparatus of claim 8, wherein the amplifier transistor (21) and the reset transistor (14) are formed in the second pixel (pixel 50 of column 1 and row C; a portion of 21 and 14 are in the second pixel) and a drain (the upper source/drain region) of the reset transistor (14) is a source (the lower source/drain region) of the amplifier transistor (21; 21 and 14 share one source/drain region).

21. Regarding **claim 15**, Guidash also teaches a solid-state imaging apparatus (image sensor; Abstract) comprising: a substrate (semiconductor substrate; Abstract); a first pixel (pixel 40 of column 1 and row A; Fig. 5, col. 4 line 31) formed on the substrate (Abstract) including a first photodiode (42 in the first pixel; Fig. 5, col. 4 line 33), a first transfer transistor (the transistor formed with the transfer gate 43 in the first pixel; Fig. 5, col. 4 line 34) and a first floating diffusion (45 in the first pixel; Fig. 5, col. 4 lines 34-35); a second pixel (pixel 40 of column 1 and row B; Fig. 5, col. 4 line 31) formed on the substrate (Abstract) adjacent to the first pixel (40 of column 1 and row B) including a second photodiode (42 in the second pixel; Fig. 5, col. 4 line 33), a second transfer transistor (the transistor formed with the transfer gate 43 in the second pixel; Fig. 5, col. 4 line 34) and a second floating diffusion (45 in the second pixel; Fig. 5, col. 4 lines 34-35); a reset transistor (14; Fig. 5, col. 4 line 35) formed on the substrate (Abstract); and an amplifier transistor (source follower input signal transistor 21; Fig. 5, col. 4 line 38) formed on the substrate (abstract), wherein a gate electrode of the amplifier transistor (the gate of 21) is connected to the first floating diffusion (45 in the first pixel; see Fig. 5 and col. 4 lines 45-48)

and the second floating diffusion (45 in the second pixel; see Fig. 5 and col. 4 lines 45-48), a source (16; Fig. 5, col. 4 lines 50-53) of the reset transistor (14) is connected to the first floating diffusion (45 in the first pixel; Fig. 5, col. 4 lines 50-53) and the source (16) of the reset transistor (14) is connected to the second floating diffusion (45 in the second pixel; Fig. 5, col. 4 lines 50-53), and the first transfer transistor (the transistor formed with the transfer gate 43 in the first pixel) and the amplifier transistor (21) are formed parallel to each other with respect to the longest edge (the longest vertical oriented edge of the gate in Fig. 5) of each of the first transfer transistor (the transistor formed with the transfer gate 43 in the first pixel) and the amplifier transistor (21; see Fig. 5, both longest edges of the gates TG1a and SIG are parallel to each other).

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

24. **Claims 16-18 and 20-22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Guidash as applied to claims 8 and 15 above, and further in view of Toyoda et al. (US 2004/0147068 A1) as can be understood since claims 8-13 and 15-23 have been rejected under 35 U.S.C. 112.

Guidash also teaches, regarding to **claims 16-17 and 20-21**, a first output interconnect (conductive interconnect layers 55 or 44; Figs. 5 and 6, col. 4 line 48 and col. 5 line 65) and a second output interconnect (VDD contact or voltage supply 8; Figs. 5 and 6, col. 3 line 60 and col. 4 lines 37), and regarding to **claims 18 and 22**, a power supply contact (VDD contact or voltage supply 8; Figs. 5 and 6, col. 3 line 60 and col. 4 lines 37); and an output contact (the source/drain contact of the row select gate transistor 30 with a row select gate (RSG) 31; Figs. 5 and 6, col. 3 line 62 and col. 4 lines 38-39).

Guidash does not teach, regarding to **claims 16 and 20**, a first output interconnect formed as a first-level metal interconnect; and a second output interconnect formed as a second-level metal interconnect, regarding to **claims 17 and 21**, the first output interconnect and the second output interconnect are aluminum interconnects, and regarding to **claims 18 and 22**, a power supply contact is a tungsten plug; and an output contact is a tungsten plug.

In the same field of endeavor of CMOS imager, Toyoda et al. teach a first interconnect (contact plug 18 in contact hole 7 and first layer aluminum film 19; paragraph [0027, 0028]) formed as a first-level metal interconnect (i.e. the lowest contact and metal levels); and a second interconnect (contact plug 18 in contact hole 17 and second layer aluminum film 20; paragraph [0029]) formed as a second-level metal interconnect (i.e. the second lowest contact and metal levels), regarding to **claims 17 and 21**, the first interconnect (7 and 19) and the second

interconnect (17 and 20) are aluminum interconnects (19 and 20 are aluminum films; paragraph [0029]), and regarding to **claims 18 and 22**, contacts (tungsten plugs 18 in contact holes 7; Fig. 1, paragraph [0028]) are tungsten plugs (paragraph [0028]).

Toyoda et al. also teach that the aluminum interconnects and tungsten plugs are for connecting terminals of the devices (paragraph [0028-0029])

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Guidash and Toyoda et al. and use the first and second interconnects as either the first output interconnect or the second output interconnect, and tungsten plugs as the power supply contact and the output contact taught by Toyoda et al., because the aluminum interconnects and tungsten plugs are for connecting terminals of the devices as taught by Toyoda et al. (paragraph [0028-0029]). Using the first-level metal interconnect as the first output interconnect and the second-level metal interconnect as the second output interconnect is a design choice.

25. **Claims 19 and 23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Guidash as applied to claims 8 and 15 above, and further in view of Abramovich (US 2001/0010952 A1) as can be understood since claims 8-13 and 15-23 have been rejected under 35 U.S.C. 112.

Guidash also teaches, regarding to **claims 19 and 23**, the photodiode (52 and 42).

Guidash does not teach, regarding to **claims 19 and 23**, a microlens formed opposed to the photodiode.

In the same field of endeavor of CMOS imager, Abramovich teaches a microlens (145; Fig. 2, paragraph [0022]) formed opposed to the photodiode (114; Fig. 2, paragraph [0022]).

Abramovich also teach that the microlens can focus light beams onto the photodiode (paragraph [0022]).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Guidash and Abramovich and use the microlens taught by Abramovich, because the microlens can focus light beams onto the photodiode as taught by Abramovich (paragraph [0022]).

Response to Arguments

26. Applicant's amendments, filed 07/27/2009, overcome the rejections to claims 8-13 under 35 U.S.C. 112. The rejections to claims 8-13 under 35 U.S.C. 112 have been withdrawn.

27. Applicant's arguments with respect to claims 8-13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsin-Yi (Steven) Hsieh whose telephone number is 571-270-3043. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811

/H. H./
Examiner, Art Unit 2811
9/29/2009